ABSTRACT OF THE DISCLOSURE

A dual-mode dual-data rate (DDR) synchronous dynamic random access memory (SDRAM)/synchronous graphic random access memory (SGRAM). An exemplary DDR SDRAM/SGRAM comprises a single memory device, which itself comprises a memory array including a quad-bank DRAM and a logic circuitry. The logic circuitry is coupled to the memory array and is configurable to operate the single memory device in a first mode and a second mode. The first mode may include a delayed lock loop (DLL) capability while the second mode may include a non-DLL capability.